PATENT NO. : 7,071,557 B2 Page 1 of 5

APPLICATION NO.: 09/388031 DATED: July 4, 2006 INVENTOR(S): Salman Akram

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page showing the illustrative figure should be deleted to be replaced with the attached title page.

The drawing sheets, consisting of Figs. 3a, 3b and 5, should be deleted to be replaced with the drawing sheets, consisting of Figs. 3a, 3b and 5, as shown on the attached pages.

COLUMN 7, LINE 52, change "for sec ond" to --for second--

CLAIM 45,

COLUMN 12, LINE 47, change "The structure of claim 41," to --The structure

of claim 44,--

Signed and Sealed this

Twenty-second Day of December, 2009

David J. Kappos Director of the United States Patent and Trademark Office

Varid J. Kappos

(12) United States Patent

METALLIZATION STRUCTURES FOR

(54) METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS, METHODS FOR MAKING SAME, AND SEMICONDUCTOR DEVICES INCLUDING SAME

- (75) Inventor: Salman Akram, Boise, ID (US)
- (73) Assignee: Micron Technology, Inc., Boise, ID
- (*) Notice:

This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154 (a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

- (21) Appl. No.: 09/388,031
- (22) Filed: Sep. 1, 1999
- (65) Prior Publication Data

US 2002/0056914 A1 May 16, 2002

(51) Int. Cl.

H01L 23/52 (2006.01)

See application file for complete search history.

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(10) Patent No.:

US 7,071,557 B2

(45) Date of Patent:

*Jul. 4, 2006

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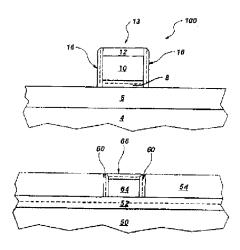
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Primary Examiner—Eugene Lee (74) Attorney, Agent, or Firm—TraskBritt

(57) ABSTRACT

The present invention provides a metallization structure for semiconductor device interconnects such as a conductive line, and methods for making the same, wherein the metallization structure includes a substrate with a substantially planar upper surface, a foundation metal layer disposed on a portion of the substrate upper surface, a primary conducting metal layer overlying the foundation metal layer, and a metal spacer on the sidewalls of the primary conducting metal layer and the foundation metal layer. The present invention also provides a metallization structure and a method for making the same, wherein the metallization structure includes a substrate with a foundation metal layer disposed thereon, a dielectric layer with an aperture therethrough being disposed on the substrate, where the bottom of the aperture exposes the foundation metal layer of the substrate and a metal spacer on the sidewall of the aperture and a line or plug of a primary conducting metal filling the remaining portion of the aperture. These metallization structures are useful for reducing the incidence and severity of thermally induced stress voids.

52 Claims, 9 Drawing Sheets



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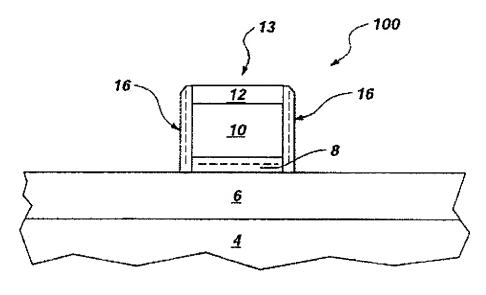


Fig. 3a

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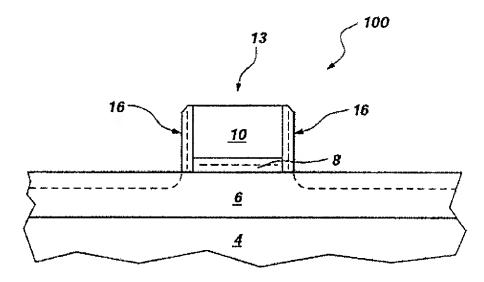


Fig. 3b

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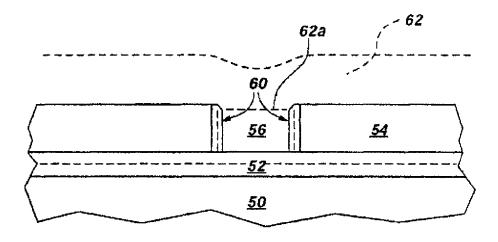


Fig. 5